REMARKS

In response to the Official Action of July 26, 2006, claims 1, 2, 5 and 8-10 have been amended, claim 6 is canceled and claims 11-17 are newly presented.

Claim 6 has been canceled since the subject matter thereof is incorporated in amended claim 1. Similar amendment has been made to electronic device claim 10. New claim 16 is similar to claim 10 but written using means-plus-function terminology.

In addition, a Replacement Sheet for Figure 3 is enclosed since the original shading with regard to a portion of said figure made reading of the underlying characters difficult. No new matter is presented in this Replacement Sheet.

Referring now to paragraphs 2 and 3 of the Official Action, claims 2, 5 and 6 are rejected under 35 USC §112, second paragraph as being indefinite for reasons set forth therein. The antecedent basis rejection for claim 2 has been corrected by positively reciting the phrase "execution of said blocks". Claim 5 has been amended to positively recite that it is the "at least two basic blocks" whereto said longest sequence belongs. This phrase finds antecedent basis in amended claim 1. Claim 6 has been canceled.

Referring now to paragraphs 4 and 5 of the Official Action, claim 8 has been amended in a manner which now positively recites a computer program product comprising code stored on a readable medium for execution by a processing unit so as to carry out the method of claim 1. Support for this amendment is found in the original application as filed, including Figure 6 and the accompanying description at page 8, line 29 through page 9, line 9. Claim 8 is therefore believed to be in compliance with 35 USC §101.

Claim 9, although not rejected under 35 USC §101, has been amended to positively recite a computer executable program which is carried by the carrier medium.

Referring now to paragraphs 6 and 7 of the Official Action, claims 1-10 are rejected under 35 USC §102(a) as anticipated in view of Sutter et al., "Sifting out the Mudd: Lower Level C++ Code Reuse" (hereinafter Sutter).

With regard to claim 1, it is recited that Sutter discloses a method for procedural abstraction comprising steps as set forth at page 4 of the Official Action. Although Sutter discloses traversing through basic blocks in order to find and abstract identical instruction sequences, such as discussed in Chapter 4.3, it does not appear in Sutter that disclosure is set forth for generating a similar function created using the longest sequence of last instruction sequences, said function then including multiple reference points within the longest instruction sequence that basically define the function from start to end.

In particular, claim 1 has been amended to particularly point out and claim the creation of a function including a longest sequence of last instruction sequences common to at least two basic blocks, wherein the longest sequence is from a plurality of sequences of last instruction sequences common to said at least two basic blocks and having a common instruction sequence of equal or shorter length as compared to the longest sequence and further that the longest sequence includes the equal or shorter length sequences of said plurality of sequences. Support for this amendment is found in Figures 2-4 and the flow chart set forth in Figure 5, as well as the accompanying description of these figures at page 5,line 17 through page 8, line 27.

With regard to claim 6, now incorporated in claim 1, the Office references Section 4.3 of Sutter, in particular, the first two sentences of the first paragraph of said section. However, neither this passage in Sutter nor the remaining discussion therein discloses claim 1 as amended and specifically the creation of a function that includes a longest sequence of last instruction sequences common to at least two basic blocks, wherein said longest sequence is from a plurality of sequences of the last instruction sequences common to said at least two basic blocks and having a common instruction sequence of equal or shorter length compared to said longest sequence, wherein the longest sequence includes the equal or shorter length sequences of said plurality of sequences and, wherein the original occurrences of instruction sequences in said plurality of sequences are replaced with a reference to a proper position in said created function.

Thus, provided that the instruction sequences are merged into a single function as set forth in amended claim 1 and that the single function represents the last instructions

of the corresponding basic blocks, the function can always be executed to the end from the utilized jump-in point (proper position). This is a beneficial feature of the invention since no further branching is required within the function.

In short, it is submitted that although Sutter mentions that previous research on abstracting partially matched basic blocks have involved restores for callee-saved registers, there is no specific disclosure for creating a function as recited above which includes a longest sequence of last instruction sequences common to at least two basic blocks, said longest sequence from a plurality of sequences of last instruction sequences common to said at least two basic blocks and having a common instruction sequence of equal or shorter length compared to said longest sequence, wherein the longest sequence includes the equal or shorter length sequences of said plurality of sequences. It also does not disclose replacing the original occurrences of said instruction sequences in said plurality of sequences with a reference to a proper position in such a created function.

Since claim 1 is therefore believed to be not anticipated by Sutter, it is respectfully submitted that dependent claims 2-5, 7 and 9 are also not anticipated by Sutter.

Claim 8 is also believed to be not anticipated by Sutter since it incorporates limitations set forth in amended claim 1 although now written in independent form.

Similarly, electronic device claim 10 is directed to a device which includes a processing unit, a memory for storing instructions and data and a data transfer module for accessing data (support is found in the application as filed, including Figure 6 and the accompanying description at page 8, line 29 through page 9, line 9), wherein the device is arranged to create a control flow graph of a computer program having instruction sequences, said control flow graph including basic blocks of instructions and wherein the device is further arranged to traverse through the basic blocks in order to detect multiple occurrences of a same instruction sequence and thereby create a function, including a longest sequence of last instruction sequences common to said at least two basic blocks. It therefore recites limitations similar to method claim 1 and, for similar reasons, is believed to be not anticipated by Sutter.

New claim 16 is similar to amended claim 10 but written using means-plus-function terminology. It is submitted that claim 16 is not anticipated by Sutter for the same reasons presented above with respect to claims 1 and 10. Claims 11-15 and 17 respectively depend from claims 10 and 16 and are therefore believed to be further not anticipated by Sutter.

In view of the foregoing amendment and discussion, it is respectfully submitted that the present application is in condition for allowance and such action is earnestly solicited.

Respectfully submitted,

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Alfred A. Fressola
Attorney for Applicant
Reg. No. 27,550

WARE, FRESSOLA, VAN DER SLUYS
& ADOLPHSON LLP
Bradford Green, Building Five
755 Main Street, P.O. Box 224
Monroe, CT 06468
Telephone: (203) 261-1234
Facsimile: (203) 261-5676
USPTO Customer No. 004955